

## DAFTAR ISI

<b>Lembar Judul</b> .....	i
<b>Lembar Pengesahan</b> .....	ii
<b>Abstract</b> .....	iii
<b>Abstraksi</b> .....	iv
<b>Kata Pengantar</b> .....	v
<b>Daftar Isi</b> .....	vi
<b>Daftar Gambar</b> .....	ix
<b>Daftar Tabel</b> .....	x
<b>Daftar Simbol</b> .....	xi
<b>Bab I Pendahuluan</b> .....	1
1.1 Latar Belakang.....	1
1.2 Perumusan Masalah.....	2
1.3 Batasan Masalah.....	2
1.4 Tujuan Penelitian.....	3
1.5 Metodologi Pemecahan Masalah.....	3
1.6 Sistematika Penulisan.....	4
<b>Bab II Landasan Teori</b> .....	5
2.1 Deskripsi Bluetooth.....	5
2.2 Enkripsi Bluetooth.....	5
2.3 Proses Enkripsi Bluetooth.....	6
2.4 Engine Enkripsi.....	7
2.4.1 LFSR dan SR (Shift Register).....	9
2.4.2 Datapath 2 Bit dan Penjumlahan Mod 2.....	11
2.4.3 Main Control.....	11
2.4.4 Shuffle Control.....	12
2.4.5 Counter 8 Bit.....	13
<b>Bab III Perancangan Sistem Engine Enkripsi Bluetooth</b> .....	14
3.1 Perancangan Engine Enkripsi Bluetooth.....	14

<b>Bab IV Implementasi, Pengujian dan Analisis Hasil Simulasi Desain.....</b>	<b>20</b>
4.1 Implementasi Verilog HDL Engine Enkripsi Bluetooth.....	20
4.2 Pengujian dan Analisis Hasil Simulasi Desain.....	21
4.2.1 Main Control.....	21
4.2.2 Shuffle Control.....	24
4.2.3 Datapath.....	26
4.2.4 LFSR1.....	28
4.2.5 LFSR2.....	30
4.2.6 LFSR3.....	32
4.2.7 LFSR4.....	34
4.2.8 Counter 8 Bit.....	36
4.2.9 Output Bit Stream.....	38
<b>Bab V Kesimpulan dan Saran.....</b>	<b>41</b>
5.1 Kesimpulan.....	41
5.2 Saran.....	41
<b>Daftar Pustaka.....</b>	<b>xii</b>
<b>Lampiran A Delay Pin ke Pin</b>	
A.1 Main Control	
A.2 Shuffle	
A.3 Datapath	
A.4 LFSR1	
A.5 LFSR2	
A.6 LFSR3	
A.7 LFSR4	
A.8 Counter 8 Bit	
A.9 Output Bit Stream	
<b>Lampiran B Source Code Verilog HDL</b>	
B.1 Control.v	
B.2 Shuffle.v	
B.3 Datapath.v	
B.4 LFSR1.v	

- B.5 LFSR2.v
- B.6 LFSR3.v
- B.7 LFSR4.v
- B.8 Counter8.v
- B.9 Synth\_top.v