ABSTRACT

Along with technological development, the more widespread use of digital imagery in various fields, such as in medicine, telecommunications, and art. In the field of telecommunications, some applications relating to digital images this is a video conferencing system (video conferencing system), remote security cameras, multimedia messaging services (multimedia messaging service), and so forth. However, the amount of information contained in digital images for these services on a large enough if we compare with the available bandwidth in the transmission of wireless communications. In addition, the storage media contained in the market was also limited. Therefore, we need a way to reduce the storage capacity without reducing image quality.

Image processing using the two-dimensional Discrete Wavelet Transformation has evolved as an effective and powerful tool in many applications, especially in image processing and compression. This is due to an efficient computational process is achieved by a factor of wavelet transforms into lifting steps. Lifting scheme facilitates high-speed and efficient implementation of wavelet transform and attract both the high throughput and low power in applications.

System Encoder Decoder image sequence as outlined in the VHDL code can be simulated and work according to specifications. Viewing sample data from the first reconstruction results, the hardware works with a value of MSE at 2135.915 and terekonstruksi image PSNR value 14.83 dB obtained for the sample while the second image obtained MSE values of 3708.298 and the values obtained PSNR is 12.43906 . VHDL code can be synthesized built and implemented on an FPGA with XST-3S1000 FPGA resources used by 65%. Given the maximum usable frequency of 116.471 MHz, this hardware can use the system clock is available on the XST-3S1000 board is 100 MHz.