

## DAFTAR ISI

<b>ABSTRAKSI .....</b>	i
<b>ABSTRACT .....</b>	ii
<b>KATA PENGANTAR .....</b>	iii
<b>DAFTAR ISI .....</b>	v
<b>DAFTAR GAMBAR .....</b>	viii
<b>DAFTAR TABEL .....</b>	x
<b>DAFTAR ISTILAH .....</b>	xi

### **BAB I PENDAHULUAN**

1.1 Latar belakang.....	1
1.2 Tujuan penulisan.....	2
1.3 Rumusan masalah.....	2
1.4 Batasan masalah.....	3
1.5 Metode penelitian.....	3
1.6 Sistematika penulisan.....	3

### **BAB II DASAR TEORI**

2.1 DFT.....	5
2.1.1 Algoritma FFT Declimation in Time dengan Radix 2 butterfly	5
2.1.2 <i>Inverse DFT</i> .....	6
2.2 FPGA Xilinx Virtex4.....	7
2.2.1 <i>Development Board</i> .....	8
2.3 HDL.....	8
2.3.1 VHDL.....	9
2.3.1.1 <i>Library</i> .....	9
2.3.1.2 <i>Entity</i> .....	10
2.3.1.3 <i>Architecture</i> .....	10
2.3.2 Verilog.....	10

2.4 32 bit floating point.....	11
--------------------------------	----

### **BAB III PERANCANGAN DAN IMPLEMENTASI**

3.1 Perancangan.....	14
3.1.1 Block serial to Paralel .....	14
3.1.2 Block IDFT .....	15
3.1.2.1 Master control.....	17
3.1.2.1.1 Control generator.....	17
3.1.2.1.2 Main Control.....	17
3.1.2.2 Address Generator Unit (AGU).....	18
3.1.2.2.1 Butterfly Generator.....	19
3.1.2.2.2 Stage Generator.....	19
3.1.2.2.3 IOD stage.....	20
3.1.2.2.4 IO address generator.....	20
3.1.2.2.5 Base Index generator.....	20
3.1.2.2.6 Shifter.....	20
3.1.2.3 Butterfly Process.....	21
3.1.2.3.1 L_block & R_block.....	22
3.1.2.3.2 Mux.....	23
3.1.2.3.3 Negate.....	23
3.1.2.3.4 Multiply.....	23
3.1.2.3.5 Adder.....	23
3.1.2.4 Cycle Unit.....	24
3.1.2.5 Coefficient ROM & Rom address generator.....	25
3.1.2.6 RAM.....	25
3.1.2.7 Counter.....	26
3.1.3 Paralel to Serial.....	26
3.2 Simulasi dengan emulator.....	27
3.3 Implementasi pada FPGA .....	29

### **BAB IV ANALISIS HASIL RANCANGAN**

4.1 Hasil simulasi.....	30
-------------------------	----

4.2 Hasil synthesis dan implementasi.....	36
4.2.1 Standard synthesis.....	40
4.2.2 Advance synthesis.....	41
<b>BAB V KESIMPULAN DAN SARAN</b>	
5.1 Kesimpulan.....	44
5.2 Saran.....	44
<b>DAFTAR PUSTAKA.....</b>	45
<b>LAMPIRAN</b>	
<b>A. Lampiran A : Report Synthesis.....</b>	46
<b>A.1 Standard Synthesis.....</b>	46
<b>A.2 Advance Synthesis.....</b>	49
<b>B. Lampiran B : Komponen – komponen hasil synthesis.....</b>	53
<b>C. Lampiran C : Code program.....</b>	81
<b>C. 1 Program utama.....</b>	81
<b>C.2 Program test bench.....</b>	83