

ABSTRACT

In digital communication systems, the information delivery system from transmitter to receiver in fact often occur bits of error caused by noise or interference when the information through the transmission channel. Nowadays, there are many channel coding methods developed to overcome these errors. These methods are expected to give better protection to the quality of the data that will be received by the receiver. The expected protection can be the detection of errors with the occurred error correction.

BCH code is one of the encoding techniques which are the implementation of channel coding. By utilizing this code, it is expected that the error occurred bits - bits of information can be detected and corrected. BCH code used in this final project is BCH (15.7). This code uses 7 bits of data information, 15 bits of codeword, and 8 of parity bits in length. This means that the code is capable of correcting errors up to 2 bits.

Design system mentioned using VHDL(Very High Speed Integrated Circuit Hardware Description Language) language programming and implementation on target device FPGA(Field Programmable Gate Array) series Xilinx Virtex XC4VLX25. After the implementation on FPGA, we can get some conclusions. Firstly, in block encoder, it is obtained that the required resource amount is 7 slices of slice, 12 slices of flip - flops, 11 LUT of 4 input LUTs, and 1% IOB in use. Secondly, in the block decoder, it is obtained that the required resource amount is 31 slices of slice, 28 slices of flip - flops, 1% of the amount of 4 input LUTs, and 1% of IOB in use. Thirdly, in the block encoder decoder simulation system, it is obtained that the required resource amount is 1% of the slice numbers, 1% of the number of slice flip flops, 1% of 4 input LUT numbers, and 7% of the number of IOB in use.