Abstract

FPGA is a new generation of memory device, FPGA device is not famous for to be used as research tools for digital telecommunications. FPGA can build the processor memory and external memory device controller, so that the FPGA can support a digital FM receiver design testing. Inside the device there are one million logic gates, in which that logic gates can be designed by using VHDL language. FPGA prototype can provide a basis for the development of capital-based design of digital telecommunication electronics.

To develop FPGA requires an implementation of digital telecommunications equipment based test. This device testing method modifies an existing digital FM receiver ICs. The principle of the circuit is implemented into the VHDL language that has already had source code, but the source code still contains many algorithms programming error. Thus, in this final project, there is a verification of existing source coding and the addition of an analog device design, so the signal modulation frequencies can be sampled and received at FM receiver processing on FPGA-based digital radio.

In these FPGA devices testing, all blocks of communication systems in digital FM receiver can be implemented at FPGA. But FPGA need a device requires 8-bit ADC with a sampling frequency of at least 22 Mhz. The final project designs a program of digital PLL and audio codec with 48 KHz sampling frequency. Further testing will be developed to be the kit of digital- based communication systems practicum.

Keywords: Digital FM receiver, PLL digital, VHDL, FPGA.